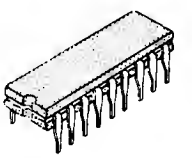
HM472114-3,HM472114-4, HM472114P-3,HM472114P-4

1024-word×4-bit Static Random Access Memory

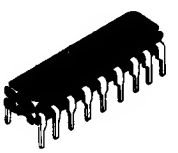
- Fast Access Time ..... HM472114-3 300ns (max.)
  HM472114-4 450ns (max.)
- Low Operating Power ..... 200mW (typ)
- Single +5V Supply Voltage
- Completely Static Memory ..... No Clock or Refresh Required
- Directly TTL Compatible ..... All Inputs and Outputs
- Common Data Inputs and Output
- Three-state Outputs
- DC Standby Mode ..... Reduces V_{CC}
- N-channel Si Gate MOS Technology
- Interchangeable with Intel 2114L Series

HM472114-3, HM472114-4



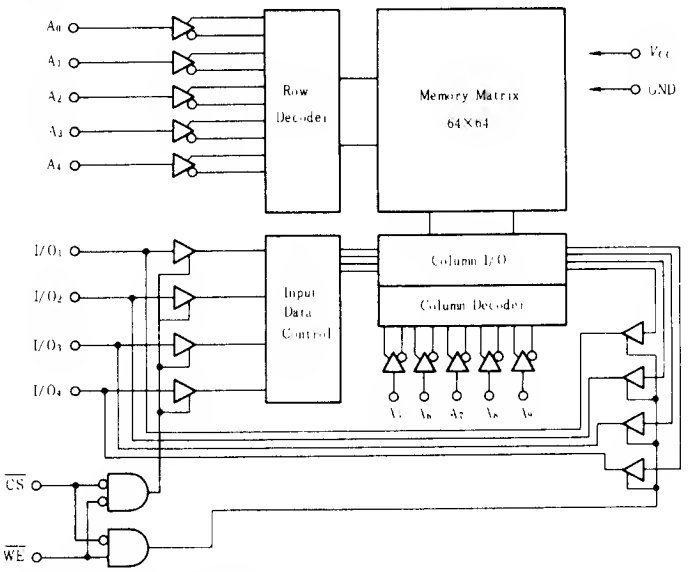
(DG-18)

HM472114P-3, HM472114P-4

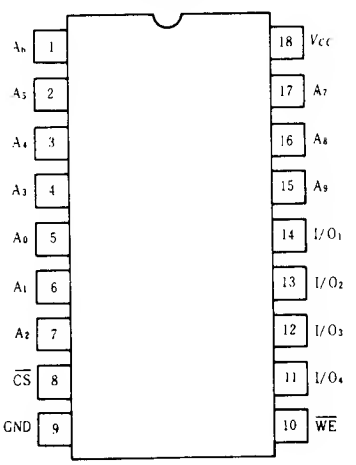


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage	V_T	−0.3 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	℃

HITACHI

■ DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=0~5.5V	—	—	10	μA
I/O Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4~V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60	mA
Input Voltage	V_{IL}		−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}= −0.6mA, V_{CC}=4.5V	2.4	—	—	V
		I_{OH}= −1.0mA, V_{CC}=4.75V	2.4	—	—	

■ CAPACITANCE (Ta=25℃, f=1MHz)

Item	Symbol	Test Condition	min.	typ.	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	10	pF

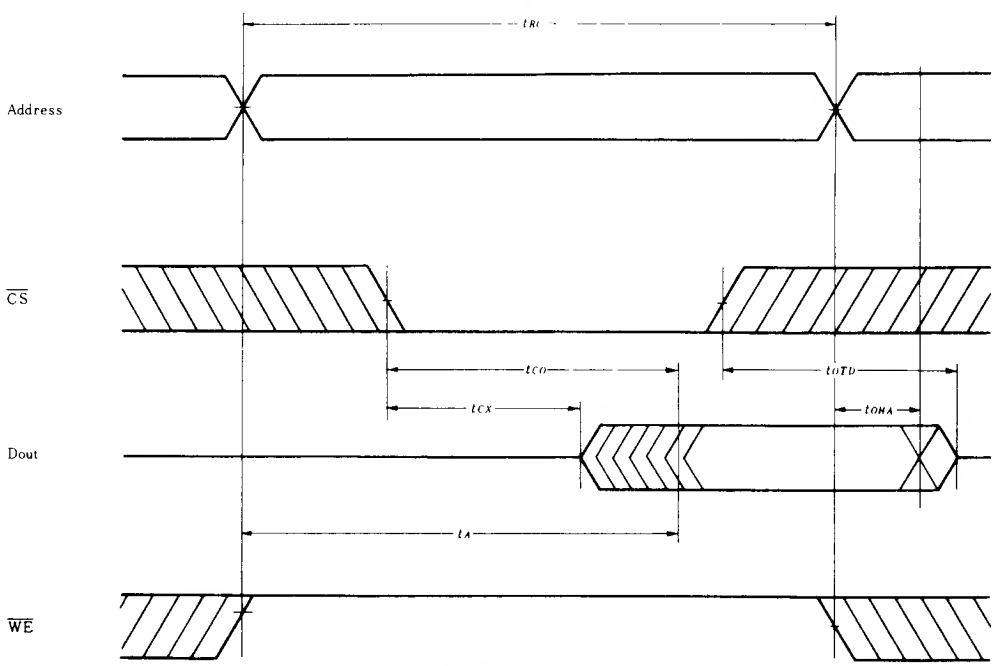
■ AC ELECTRICAL CHARACTERISTICS (Vcc=5V±10%,Ta=0 to +70°C)

• AC TEST CONDITIONS

Input High Levels 2.0V
Input Low Levels 0.8V
Input Rise and Fall Times 10ns
Input and Output Timing Levels 1.5V
Output Load ..... 1 TTL + C_L=100pF

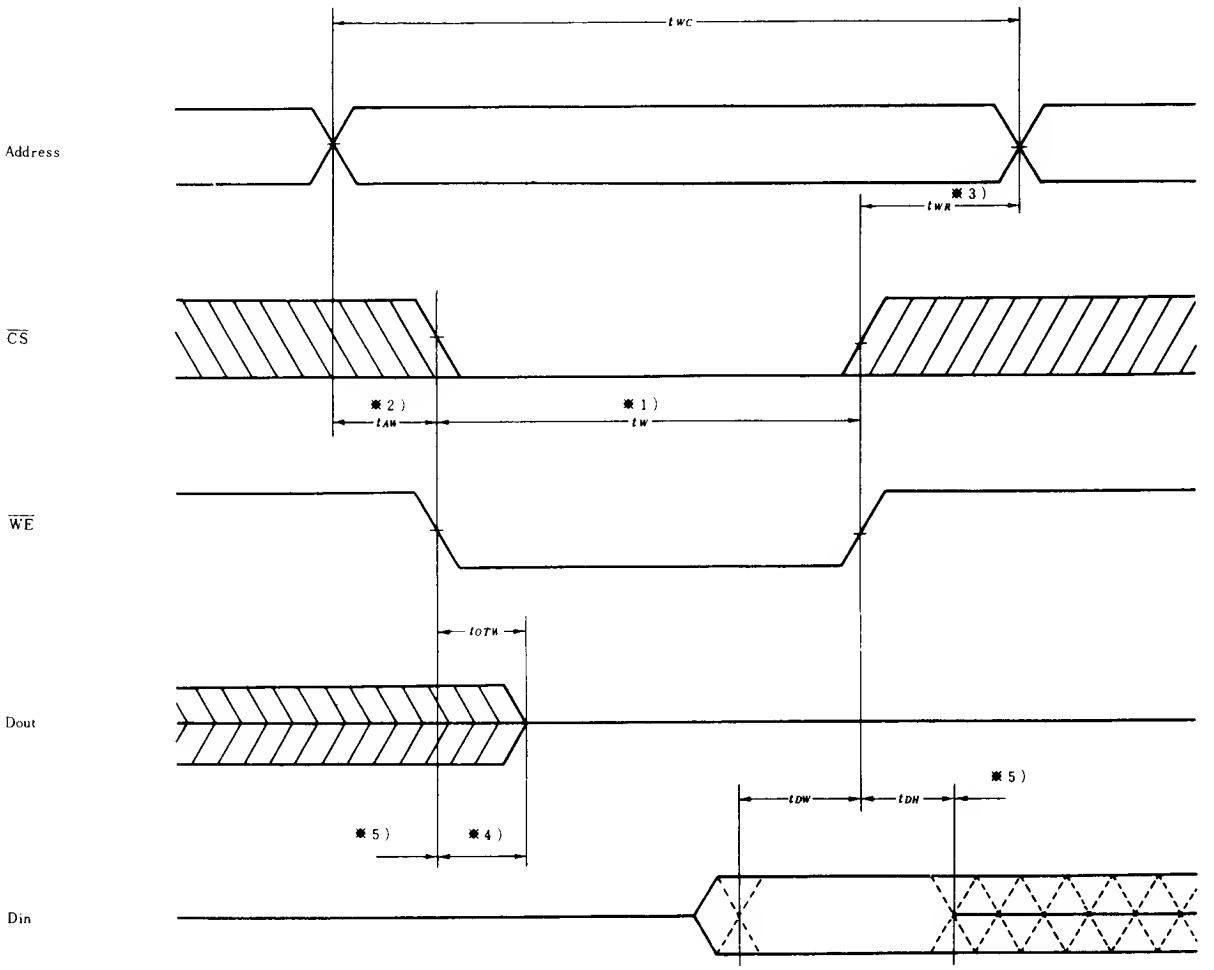
•READ CYCLE

Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	300	—	450	—	ns
Access Time	t_A	—	300	—	450	ns
$\overline{CS}$-to-Output Valid	t_{CO}	—	100	—	120	ns
$\overline{CS}$-to-Output Active	t_{CX}	20	—	20	—	ns
Output 3-state from Deselection	t_{OTD}	–	80	–	100	ns
Output Hold from Address Change	t_{OHA}	50	—	50	—	ns



■ WRITE CYCLE

Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min.	max.	min.	max.	
Write Cycle Time	t_{WC}	300	—	450	—	ns
Address to Write Setup Time	t_{AW}	20	—	50	—	ns
Write Pulse Width	t_W	150	—	200	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	–	80	–	100	ns
Data-to-Write Time Overlap	t_{DW}	150	—	200	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns



Notes: 1) $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).

2) t_{AW} is an interval from the address setting through fall of the pulse, $\overline{CS}$ or $\overline{WE}$.

3) t_W is from the earlier rise pulse of $\overline{CS}$ or $\overline{WE}$ till the end of the light cycle (t_{WC}).

4) During this period the pulse is output so that the input signal which is the same in phase with the output may be applied to the I/O terminal.

5) During this period, when the $\overline{CS}$ signal is at low level, the pulse is output so that the input signal which is the same in phase with the output data may be applied, if required. Do not however apply the input signal of reverse phase.